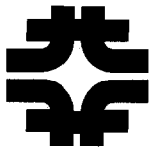

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A MEMORY-MAPPED CAMAC BRANCH DRIVER

M. F. Shea and A. A. Jones

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A Memory-Mapped CAMAC Branch Driver

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1.0 Introduction

In a distributed microprocessor-based control system, it may be necessary to interface with hardware configured in CAMAC. This note describes an interface between a VMEbus microcomputer and CAMAC.

2.0 Requirements of the CAMAC Interface

A distributed control system has a processor relatively close to actual hardware that is to be controlled. Therefore, it is not necessary to drive CAMAC crates from very remote locations, although distances of a few meters or tens of meters would be desirable. It is also desirable to minimize, or if possible, to eliminate the protocol needed to communicate with CAMAC crates.

The above requirements can be met using the Branch Highway specification and CAMAC Type A controller described in IEEE-596. This standard details the organization of multicrate systems interconnected by a parallel Branch Highway, controlled by a computer and a Branch Driver. Up to seven crates separated by a total distance of 45 meters are accomodated by this specification. All elements of this system are commercially available except the Branch Driver which is the interface between the processor and the Branch Highway. The goal of eliminating the protocol needed to communicate with CAMAC registers is achieved by mapping CAMAC registers directly into the memory space of the processor.

3.0 The Branch Driver

The Branch Driver described here is configured in VMEbus, a bus specification that uses Eurocard hardware. It was defined by Motorola, Mostek, Signetics and Phillips for use in 68000-based systems.

Figure 1 is a block diagram of the Branch Driver, but its operation is best described using Figure 2, the assignment of address bits. Mapping CAMAC registers into address space requires 3 bits for the crate number, 5 bits for slot number, 4 bits for subaddress and 4 bits for function code. The fifth function code bit ,F16, determines if the function is a read or a write. It is derived from the WRITE* line of the VMEbus.

Address bits A23...A18 are compared with the onboard 6-bit switch that determines the address block occupied by the Branch Driver. The two least significant addresses are used for byte number. Each CAMAC read and write operation involves four bytes of address space---three bytes of data and one byte of status.

Control logic on the board causes a CAMAC cycle to occur when byte zero is read and when byte three is written. Any of these registers may be read or written using the normal 68000 MOVE instructions and MOVE.B, MOVE.W and MOVE.L are all accomodated. A write cycle to a specific CAMAC register, CNAF, can be accomplished by a single MOVE.L instruction and similarly a MOVE.L instruction can read a 24 bit CAMAC register plus the status into a data register of the 68000 (or into any memory location within the 16 M-byte address range). Note that on a long word read, the status is automatically stored in the most significant byte. Following a write operation, the status word must be read separately in order to test the Q and X bits. During a CAMAC operation, the DTACK signal is derived from the BTB signal returned by the addressed Type A crate controller. In this way the processor is forced to wait for the CAMAC cycle to complete. If BTB is not returned, the VMEbus watchdog timer would cause a BUS ERROR to occur and the bus error exception processing routine would be executed to handle the condition.

In the present implementation, the Branch Demand signal is included as a bit in the status register. It could be allowed to interrupt the processor if fast response to external events is needed.

4.0 Timing

The Branch Driver design described here meets the timing requirements of the IEEE-596 standard. With settling delays and deskewing delays included, the memory cycle that causes the one microsecond CAMAC cycle is stretched to 1.4 microseconds. Figure 3A shows a timing diagram of a write and read cycle. The listing of the 68000 test routine used to exercise the branch driver is given in Figure 3B. The timing diagram results from the execution of the two "MOVE.L" instructions in lines 13 and 14.

5.0 Discussion

The Branch Driver described here has been built and operated using a Motorola VME-110 68000-based microcomputer board, a standard Type A controller and a CAMAC crate. This driver performs all the functions required by the specification except the multiple crate functions that can easily be accomodated individually.

The simplicity of addressing CAMAC registers as memory is only possible with processors that have adequate address space. A Branch Driver that controls up to seven CAMAC crates consumes one-quarter megabyte of memory space. Of course, not all addresses correspond to real registers; each slot is allocated 1024 bytes of memory, although typical CAMAC cards rarely use more than a few dozen bytes. Addresses not used by CAMAC registers are not available for other purposes, but the lost address space is the only penalty that comes from the memory-mapped organization. In the case of the 68000, the quarter-megabyte is only one sixtyfourth, less than 2%, of the available 16 Megabyte address space.

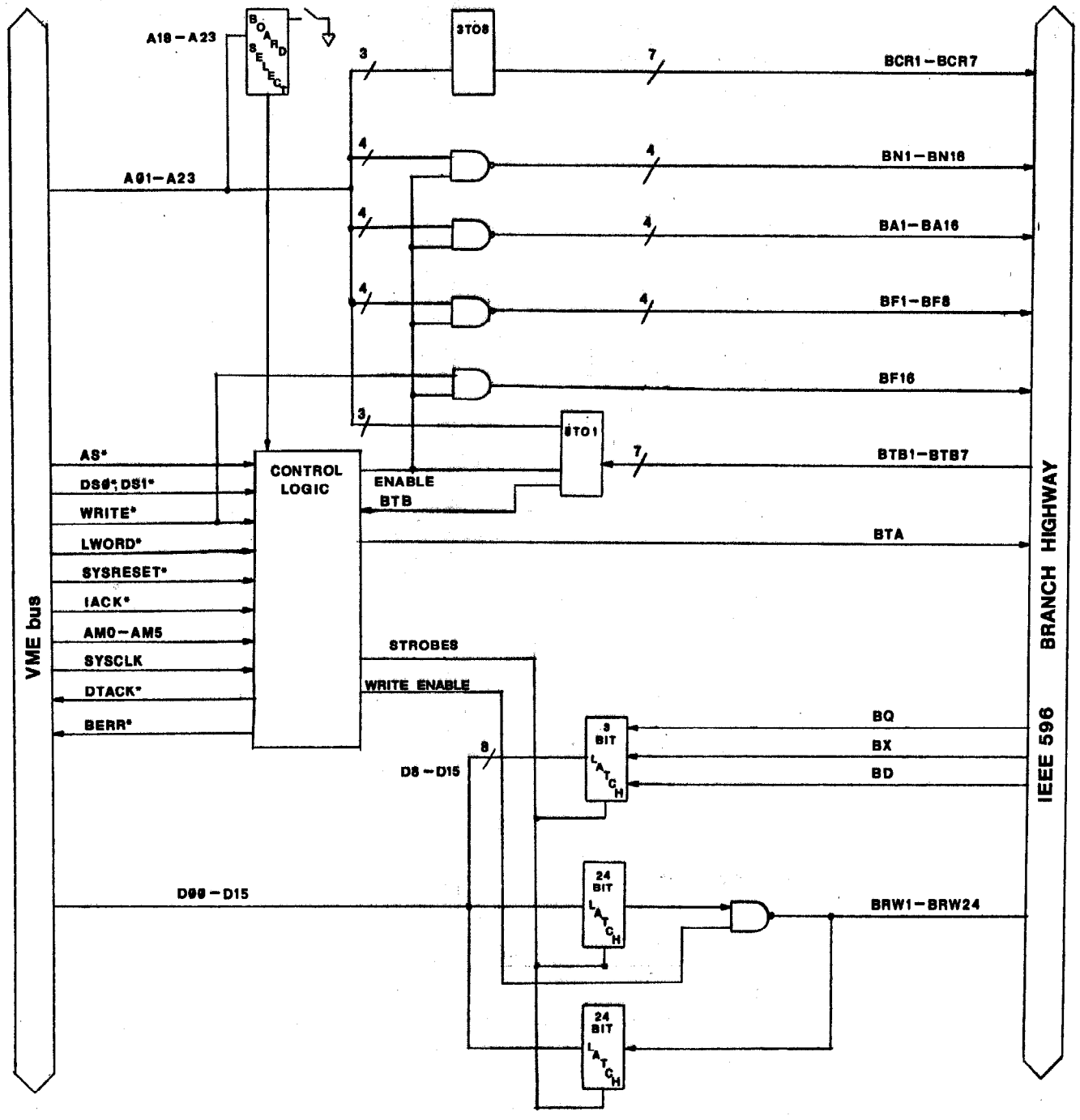


FIGURE 1

REV.	DESCRIPTION	DRAWN	DATE
		APPD.	DATE

ITEM NO.	PART NO.	DESCRIPTION OR SIZE	QTY. REQ.

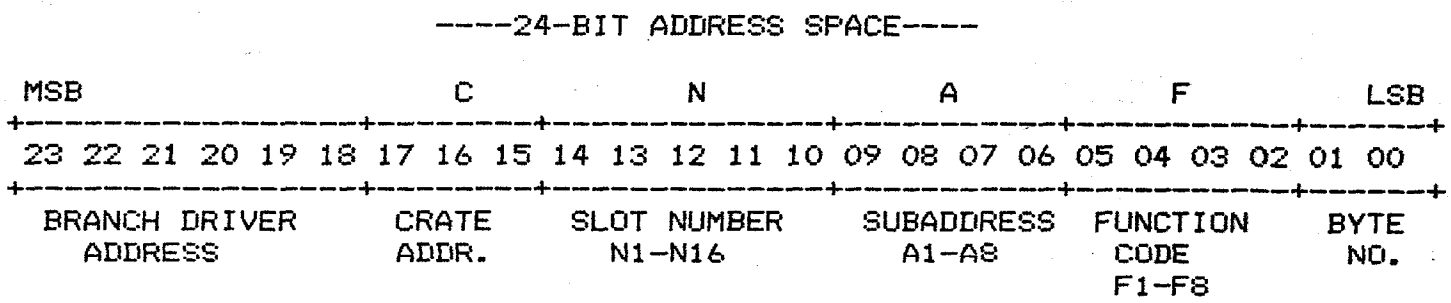
PARTS LIST

UNLESS OTHERWISE SPECIFIED			ORIGINATOR	M. SHEA	5/82
FRACTIONS	DECIMALS	ANGLES	DRAWN	R. FLORIAN	5/82
±	±	±	CHECKED		
1. BREAK ALL SHARP EDGES 1/64 MAX.			APPROVED		
2. DO NOT SCALE DWG.			USED ON		
3. DIMENSIONING IN ACCORD WITH ANSI Y14.5 STD's.			MATERIAL-		
MAX. ALL MACHINED SURFACES					

FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

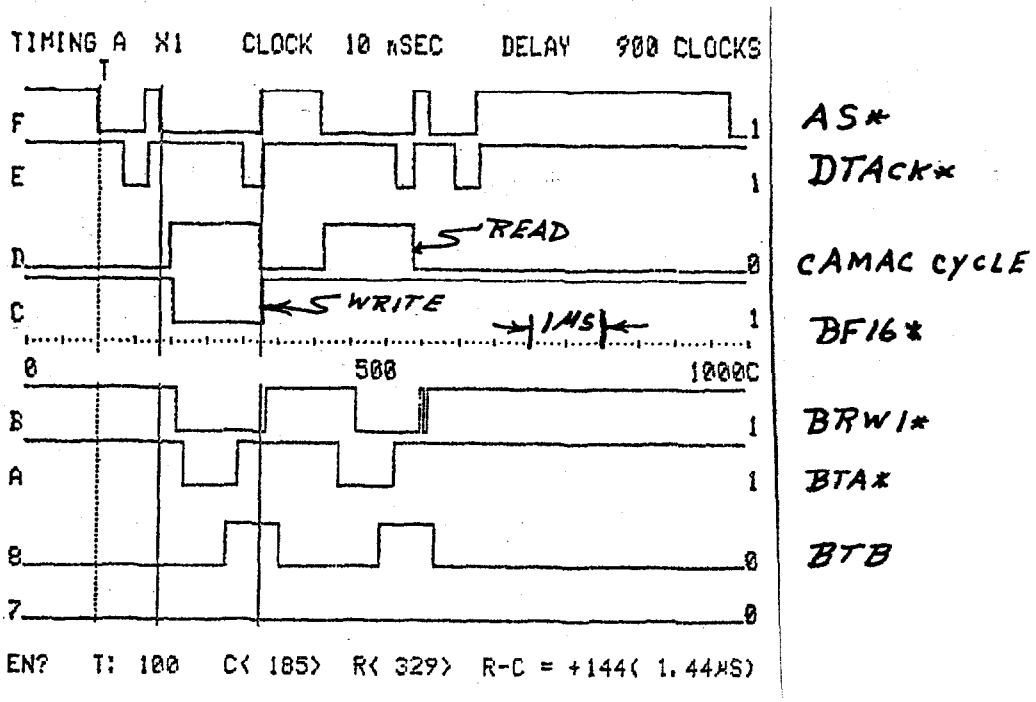
CONTROLS
VMEbus/CAMAC BRANCH DRIVER

SCALE	FILMED	DRAWING NUMBER	REV.



NOTE: F16 IS DERIVED FROM VMEBUS "WRITE*".

FIGURE 2. BIT ASSIGNMENTS FOR MEMORY-MAPPED CAMAC BRANCH DRIVER



- A -

```
MOTOROLA M68000 ASM VERSION  1.30SYS : 351,        .BRDRPROG.SA 05/17/83 15:55:04

   1                          *          ------ ------VMEBUS/BRANCH-DRIVER TEST ROUTINE---------
   2                          *
   3                          *
   4            00002000                 ORG      $2000
   5            00C10400      DISPLY     EQU      $C10400          ADDRESS OF DATAWAY DISPLAY MODULE: C2,N1,A0,F0
   6            00C11000      SWMOD      EQU      $C11000          ADDRESS OF CAMAC SWITCH INPUT MODULE: C2,N4,A0,F0
   7                          *
   8                          *
   9                          *----------------PROG TO COUNT INTO DISPLAY MODULE'S LEDS-------------
  10                          *
  11                          *
  12   00002000 227C00C10400 START1   MOVE.L   #DISPLY,A1
  13   00002006 2280         LOOP     MOVE.L   D0,(A1)          WRITE TO MODULE  } See 3(A) above
  14   00002008 2211                  MOVE.L   (A1),D1          READ FROM MODULE }
  15   0000200A 5280                  ADDQ.L   #1,D0            CHANGE THE DATA
  16   0000200C 60F8                  BRA.S    LOOP             AND REPEAT FOREVER
  17   0000200E 4E71                  NOP
  18                          *
  19                          *
  20                          *--------PROGRAM TO REPLICATE SWITCH SETTINGS IN DATAWAY DISPLAY LEDS-------
  21                          *
  22                          *
  23   00002010 207C00C10400 START2   MOVE.L   #DISPLY,A0
  24   00002016 227C00C11000          MOVE.L   #SWMOD,A1
  25   0000201C 2091         LOOP2    MOVE.L   (A1),(A0)         MOVE THE SWITCH DATA INTO THE DISPLAY MODULE
  26   0000201E 60FC                  BRA.S    LOOP2             AND REPEAT FOREVER
  27                                  END

****** TOTAL ERRORS       0--
****** TOTAL WARNINGS     0--
```

- B -

Figure 3. (A) Timing Diagram
(B) Test Program